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A Novel Six-Transistor SRAM Cell with Low Power Consumption

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Abstract: In this paper, two static random access memory (SRAM) cells that reduce the static power dissipation due to gate and sub threshold leakage currents are presented. The first cell structure results in reduced gate voltages for the NMOS pass transistors, and thus lower the gate leakage current. It reduces the sub threshold leakage current by increasing the ground level during the idle (inactive) mode. The second cell structure makes use of PMOS pass transistors to lower the gate leakage current. In addition, dual threshold voltage technology with forward body biasing is utilized with this structure to reduce the sub threshold leakage while maintaining performance. Analysis is done by comparing the power consumed by the different SRAM designs. The performance of the proposed designs can be analyzed with (1.25µm CMOS) T-spice tool. The results showed that PP-SRAM designs consumed less power compared to other designs.

Index Terms: Dual threshold, gate leakage, low-power, static power, static random access memory (SRAM) cell, tunneling current.

I. INTRODUCTION

In bulk CMOS technology, the gate -to- substrate leakage current is several orders of magnitude lower than the overlap tunnelling current and gate-to-channel current. In the ON state, in addition to the overlap tunnelling currents, the gate-to-channel tunnelling is added to the gate current increasing the total gate tunnelling current in this state. There are several techniques for reducing the gate tunnelling leakage in digital circuits. These techniques reduce the leakage based on the dependencies of the tunnelling currents on the terminal voltages, the gate oxide thickness, and the type of the transistor. One of the techniques is to employ PMOS transistors instead of NMOS transistors. In the PMOS transistor, the gate tunnelling current is an order of magnitude lower than that of the NMOS transistor in the inversion regime in the same technology. We present two design techniques that reduce the gate leakage current in the SRAM cells. In both designs, we focus on the static power dissipation in the idle mode where the cell is fully powered on, but no read or write operation is performed.

II. EXISITING METHOD

1. NC-SRAM CELL

This section presents an N- Controlled SRAM (NC-SRAM) design for maxi mum leakage reduction in cache and embedded memories without affecting the performance significantly available dual -Vt and supply voltage gating techniques. The key idea of the NC-SRAM is the use of two pass-transistors that provide different ground supply voltages to the memory cell for nor mal and sleep modes. These pass- transistors provide a positive ground supply voltage when the cell is inactive and connect the cross-coupled inverters to the ground supply during nor mal operation to functionas a conventional 6T-cell. The positive voltage during the stand-by state has 3 important effects: (i) Negative body to source potential causes more body effect resulting in increased threshold (ii) Gate to source voltage becomes negative (iii) Drain to source potential decreases resulting in less Drain Induced Barrier Lowering (DIBL). These effects combined together results i n low sub-threshold and gate leakage currents. The gate leakage of the n MOS transistors in the cross-coupled inverter is reduced signicantly due to the increase in the source voltages of transistors, M3 and M4. In addition, as high-V devices are used for the access transistors that connect the memory's internal inverters to the read/write lines, the leakage through the bit lines is reduced considerably.

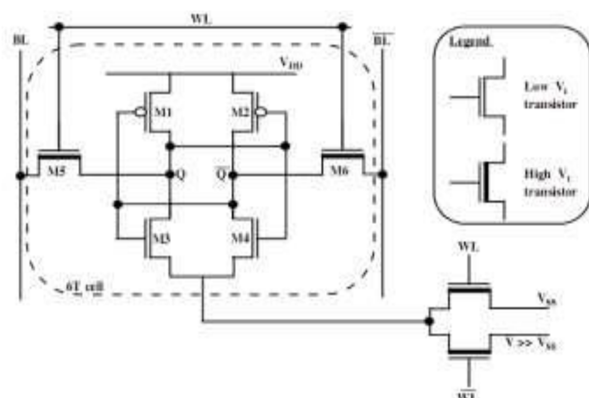

Figure 2: NC-SRAM Cell Using Pass Transistors

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The two pass transistors that control the threshold voltages of the nMOS transistors can be shared among multiple SRAM cells to reduce the area overhead. In our design, the word line from the row decoder logic are used to control the gates of these pass transistors.

2. WL-VC SRAM Cell

In this section, we present our gate leakage current reduction method based on WL Voltage Control (WL-VC).The proposed configuration of SRAM is illustrated in Fig.3. 3] In order to when the SRAM cell is in the inactive mode. To overcome this problem we Combine this method by NC-SRAM. The NC- SRAM design employs Dynamic Voltage Scaling to reduce the leakage power of the cash cells and retain the stored data during the in active mode.[2]When the cell is in the active mode, WL is 'I' and the minimum voltage is applied to the cell. In the in active mode, WL is'0', and, therefore the positive voltage V is applied to the SRAM cell through the Pass transistor.

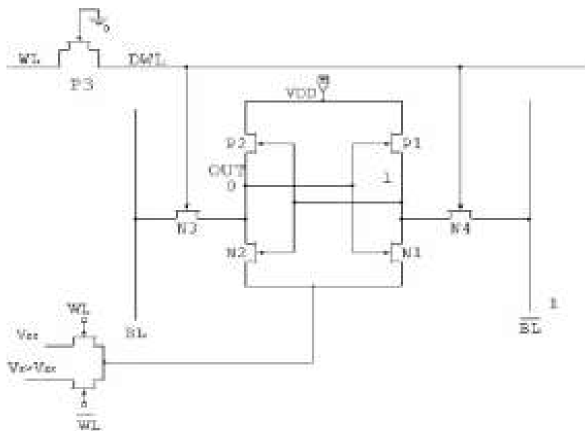

Figure 3: WL-VC SRAM cell.

3. PP-SRAM CELL

We present a gate leakage current reduction method based on PMOS Pass-transistor SRAM structure which is illustrated in Fig.4..[4] The PMOS Pass-transistor SRAM (called PP - SRAM) cell has lower gate leakage compared to that of the conventional SRAM cell. In order to decrease the gate leakage currents of the SRAM cell, NMOS transistors N3 and N4, are replaced PMOS transistors P3 and P4.

Since SL is activated before WL is activated for the read/write operation, the timing performance deterioration is prevented. It is important to point out that due to the use of the PMOS transistors, there is an increase in the dynamic power of the cell which is consumed during the read and write operation. Since static power is much more important than dynamic power in large memories, static power saving will very well compensate for the increase in dynamic power dissipation.

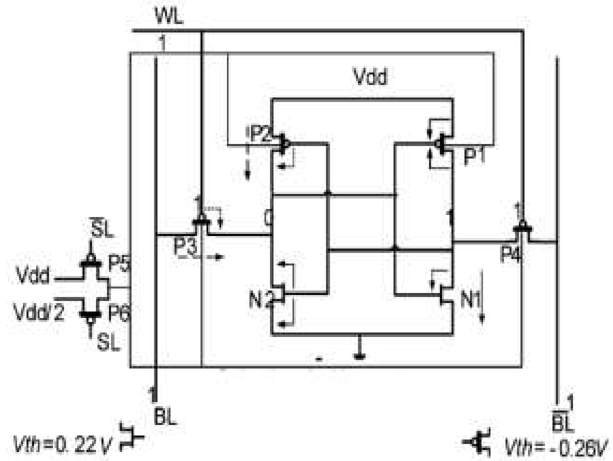

Figure 4: PP-SRAM cell

III. PROPOSED METHODS

1. 8T- PP SRAM

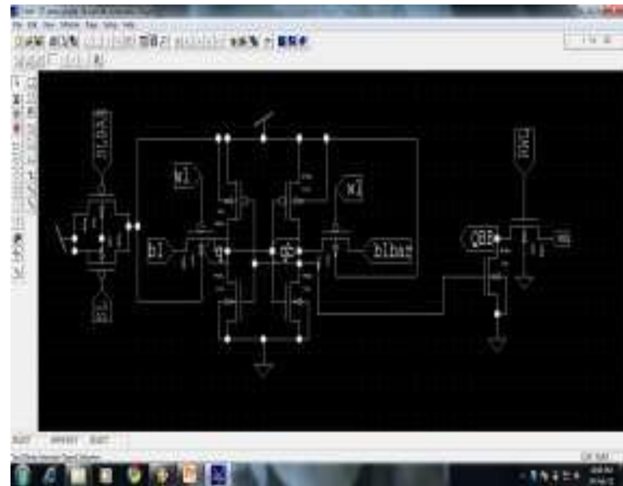

Figure 5:8T-PP-SRAM

2.9T-PP-SRAM

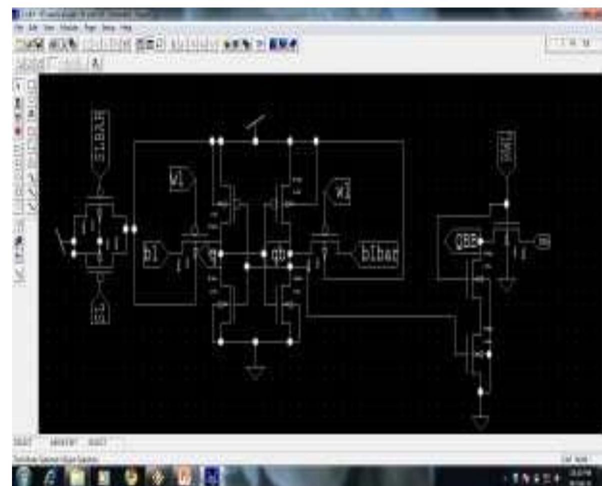

Figure 6: 9T-PP-SRAM

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3.10T-PP-SRAM

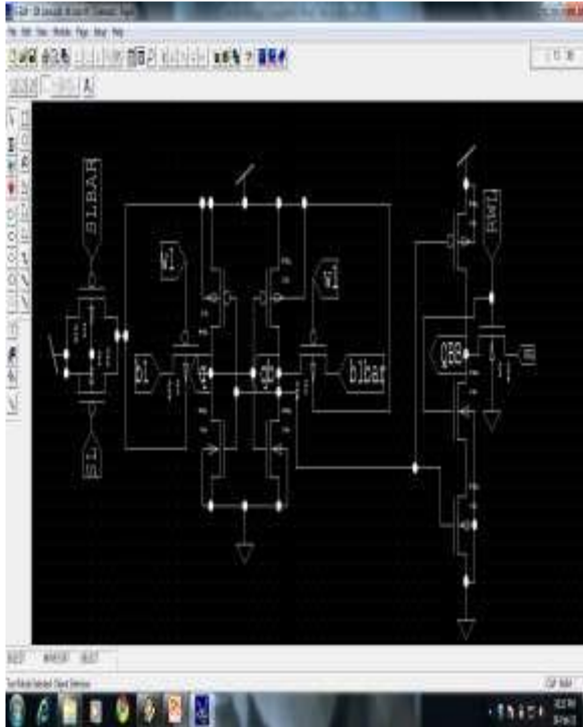

Figure 7:10T-PP-SRAM

IV.SIMULATION OUTPUT

The Figure 6 and 7 shows simulation results obtained for the PP -SRAM cell and 10T PP- SRAM cell.

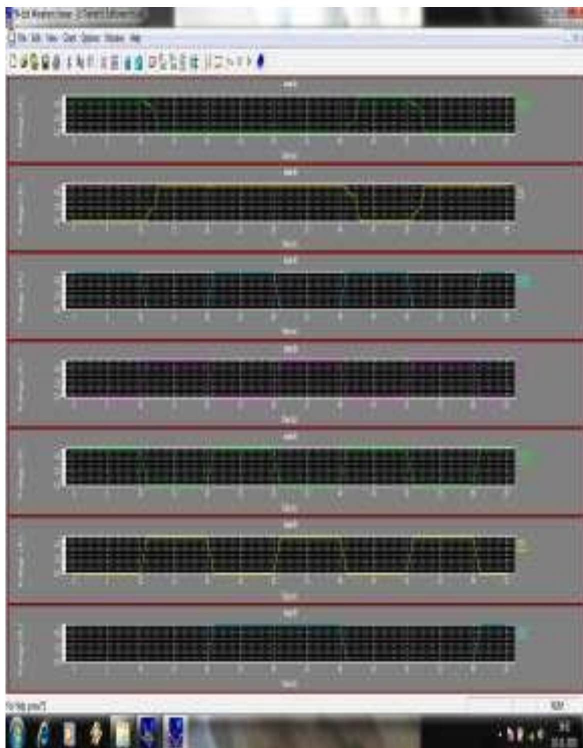

Figure 8: PP-SRAM cell output

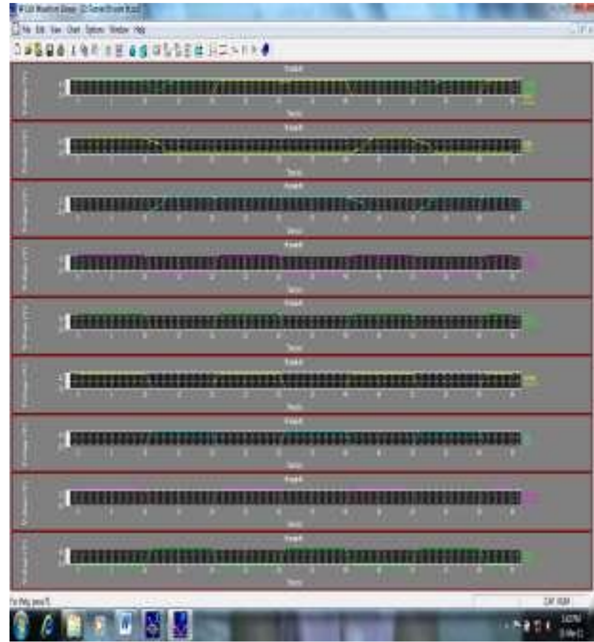

Figure 9:10T-PP-SRAM cell output

V.RESULT

The performance analysis of the proposed designs was analyzed with (1.25µm CMOS) T-spice tool. Here the power consumed by different SRAM cells was analyzed. The power consumed by different SRAM structures. The Fig: 7 shows the power consumed by SRAM cells. We an see a considerable reduction in power for the PP -SRAM structure compared to the other cell structures. Here PP -SRAM architecture can be done for further reduction in power dissipation at the expense of latency as power forms the important criteria in8T, 9T, and 10TSRAM architectures.

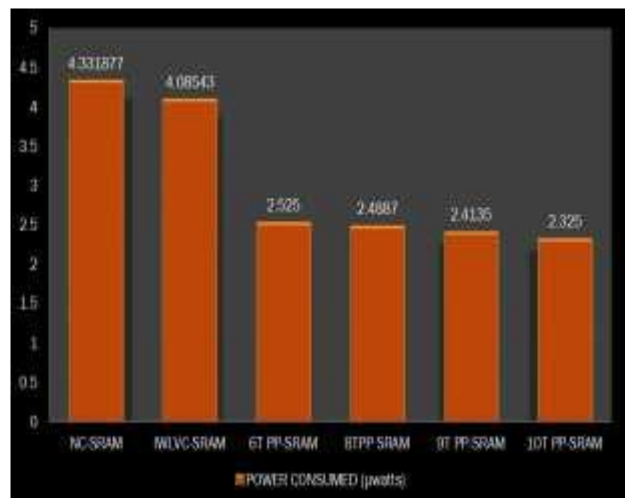

Figure 10: Power consumption of SRAM cells.

The figure 10 also shows the power consumed by the 10TSRAM cell using PP- SRAM which shows even more reduction in the power consumption.

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VI. CONCLUSION

The two new structures for the SRAM cell called IWL – VC SRAM and PP -SRAM were presented. The first cell structure made use of one PMOS per row of SRAM cells as well as two NMOS transistors for changing the ground voltage during the active and idle modes. In the second cell structure, PMOS pass transistors with high and forward biasing method were used to reduce both the gate oxide direct tunneling and the sub threshold currents. PP-SRAM showed a considerable reduction in the power consumed. A future work was carried out where a 10T SRAM cell was constructed using PP -SRAM which showed a further reduction in power dissipation at the expense of latency.

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